Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A parasitic capacitance-preventing dummy solder bump structure, the dummy solder bump structure being formed on a substrate, the dummy solder bump structure comprising:

at least one conductive layer formed on the substrate;

a dielectric layer formed on the substrate to cover the conductive layer;

an under bump metallurgy layer (UBM layer) formed on the dielectric layer; and

a solder bump formed on the UBM layer.

[c2] 2.The dummy solder bump structure of claim 1 wherein the substrate is a semiconductor wafer with circuits formed inside the semiconductor wafer, and the dielectric layer comprises at least one deposition layer formed by a chemical vapor deposition (CVD) process and employed as a passivation layer.

[c3] 3.The dummy solder bump structure of claim 2 wherein the deposition layer comprises either silicon nitride or silicon oxide.

[c4] 4.The dummy solder bump structure of claim 1 wherein the UBM layer is a metal layer formed by a sputtering process.

[c5] 5.The dummy solder bump structure of claim 1 wherein a plurality of solder bump structures is formed on the dielectric layer.

[c6] 6.The dummy solder bump structure of claim 5 wherein each of the solder bump structures comprises:
a metal pad formed on the dielectric layer;
an UBM layer formed on the metal pad; and
a solder bump formed on the UBM layer.

[c7] 7.The dummy solder bump structure of claim 6 wherein each of the solder bump structures comprises at least one via plug for electrically connecting the solder bump structure with a corresponding portion of the conductive layer below the solder bump structure.

[c8] 8.The dummy solder bump structure of claim 5 wherein the solder bump structure is positioned in a central area of a surface of the substrate, and the dummy solder bump structures are positioned in a border area of the surface of the substrate to surround at least one of the solder bump structures.

[c9] 9.The dummy solder bump structure of claim 1 wherein

the dummy solder bump structure is employed to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

[c10] 10.A method of forming a solder bump on a substrate, the substrate comprising at least one conductive layer positioned on a surface of the substrate, the surface of the substrate comprising a first area and a second area, the method comprising:
performing a CVD process to form a dielectric layer on the substrate to cover the conductive layer;
forming at least one via plug in portions of the dielectric layer within the first area down to a surface of the conductive layer;
forming at least one metal pad electrically connected to the via plug;
performing an UBM process to form at least one UBM layer to cover both the metal pad within the first area and portions of the dielectric layer within the second area; and
forming a solder bump on the UBM layer.

[c11] 11.The method of claim 10 wherein the dielectric layer comprises a passivation layer atop the dielectric layer.

[c12] 12.The method of claim 11 wherein the dielectric layer and the passivation layer comprise either silicon nitride

or silicon oxide.

[c13] 13.The method of claim 10 wherein the via plug comprises either one of titanium (Ti), titanium nitride (TiN), tungsten (W), aluminum (Al), copper (Cu) or copper-aluminum alloy (Cu-Al alloy).

[c14] 14.The method of claim 10 wherein the UBM layer is formed by performing a sputtering process.

[c15] 15.The method of claim 10 wherein the solder bump formed within the second area is employed as a dummy solder bump to improve the fluidity of an underfill liquid compound in subsequent packaging processes.

[c16] 16.The method of claim 10 wherein the substrate is a semiconductor wafer with circuits formed inside the semiconductor wafer.

[c17] The method of claim 10 wherein the first area and the second area are respectively a central area and a border area of the surface of the substrate.